AMENDMENTS TO THE CLAIMS

1. (Original) A memory cell in an array of memory cells, a memory cell comprising:

a substrate;

a floating gate formed at least in part within said substrate; and

a bit line region formed within said substrate in proximity to said floating gate.

2. (Original) The memory cell of Claim 1 wherein said bit line region lies completely within said substrate.

3. (Original) The memory cell of Claim 1 wherein said bit line is formed in proximity to two adjacent surfaces of said floating gate.

4. (Original) The memory cell of Claim 3 wherein said bit line region is located below said floating gate and along one side of said floating gate.

5. (Original) The memory cell of Claim 1 further comprising:

a dielectric layer disposed over said floating gate; and

a control gate disposed over said oxide layer.

6. (Original) The memory cell of Claim 5 wherein said substrate comprises silicon, said floating gate and said control gate comprise polysilicon, said bit line region comprises arsenic, and said dielectric layer comprises oxide-nitride-oxide.

7. (Original) The memory cell of Claim 1 further comprising:

a tunnel oxide layer formed between said substrate and said floating gate.

8. (Withdrawn) A method of forming a memory cell, said method comprising:

forming a trench in a substrate;

implanting a dopant into said substrate to form a bit line region in proximity to said trench and within said substrate; and

forming a floating gate in said trench such that said bit line region and said floating gate are in proximity.

9. (Withdrawn) The method of Claim 8 further comprising:

forming a tunnel oxide layer on surfaces of said trench prior to formation of said floating gate.

10. (Withdrawn) The method of Claim 8 further comprising:

forming a dielectric layer over said floating gate; and

forming a control gate over said oxide layer.

11. (Withdrawn) The method of Claim 10 wherein said substrate comprises silicon, said floating gate and said control gate comprise polysilicon, said bit line region comprises arsenic, and said dielectric layer comprises oxide-nitride-oxide.

12. (Withdrawn) The method of Claim 8 wherein said bit line region is buried within said substrate.

13. (Withdrawn) The method of Claim 8 wherein said bit line region is located below said trench and along one side of said trench.

14. (Withdrawn) The method of Claim 8 further comprising:

filling portions of said trench that remain after said floating gate is formed with silicon oxide.

15. (Original) A flash memory array comprising:

a plurality of floating gates arrayed in rows and columns, said floating gates formed at least in part within a substrate;

a control gate coupling floating gates and functioning as a word line; and

a bit line that is essentially perpendicular to said word line, said bit line buried within said substrate.

16. (Original) The flash memory array of Claim 15 wherein said bit line is formed in proximity to two adjacent surfaces of said floating gates.

17. (Original) The flash memory array of Claim 16 wherein said bit line is located below and along one side of said floating gate.

18. (Original) The flash memory array of Claim 15 further comprising:

a dielectric layer formed between said control gate and said floating gates.

19. (Original) The flash memory array of Claim 18 wherein said oxide layer and said control gate are formed such that they separate adjacent floating gates along said word line.

20. (Original) The flash memory array of Claim 18 wherein said substrate comprises silicon, said floating gates and said control gate comprise polysilicon, said bit lines comprise arsenic, and said dielectric layer comprises oxide-nitride-oxide.

21. (Original) The flash memory array of Claim 15 further comprising:

a tunnel oxide layer formed between said substrate and said floating gates.